REMARKS

The Examiner is thanked for the thorough examination of the present application. The FINAL Office Action, however, tentatively rejected all pending claims: 1-19, 26, and 27. Specifically, claims 1-19, 26 and 27 are rejected under 35 U.S.C. 103(a) as allegedly unpantable over Johnson (US 6,525,953) in view of Chakrabarti et al. (US 5,747,135).

In response, Applicants have amended independent claims 1 and 14 to more clearly define a novel and non-obvious aspect of the claimed embodiments. Bases for the amended claims can be found throughout the specification, drawings and claims of the original application. For example, the amendment to claims 1 and 14 is clearly supported by the specification at, for example, page 13, the first paragraphs from the top of the page and FIG. 6. Accordingly, these amendments add no new matter to the application. Reconsideration and withdrawal of claim rejections are respectfully requested in light of the amendments and following remarks.

Claim Rejections - Under 35 USC §103

Independent Claim 1

As amended herein, claim 1 defines:

> 1. A method of fabricating a semiconductor memory device comprising:
> providing a substrate;
> sequentially forming a first conductive layer, a first type doped semiconductor layer, a first dielectric layer, a second type doped semiconductor layer on the substrate;
> patterning the second type doped semiconductor layer, the first dielectric layer, the first type doped semiconductor layer, and the conductive layer along the first direction, thereby turning the conductive layer into a first conductive line;
> ***etching the second type doped semiconductor layer, the first dielectric layer, and the first type doped semiconductor layer into a***

memory cell causing particulate silicon residues on the surface of the first conductive line;

depositing a second dielectric layer overlying the substrate, wherein oxygen plasma sputtering is employed to oxidize and remove the particulate silicon residues on the surface of the first conductive line before deposition;

planarizing the second dielectric layer to expose the memory cell; and

forming a second conductive line overlying the second dielectric layer, running generally orthogonal to the first conductive line.

(*Emphasis added.*) Claim 1 patently defines over the cited art for at least the reason that the cited art fails to disclose those features emphasized above.

As the Examiner acknowledges in the Office Action, Johnson does not disclose employing oxygen plasma sputtering to clean the substrate before deposition of a layer. More specifically, Applicants respectfully submit that Johnson fails to disclose, teach or suggest that particulate silicon residues, due to etching process, are oxidized and removed by oxygen plasma sputtering before deposition of a second dielectric layer.

Moreover, Applicants respectfully submit that ***the memory device*** taught by Chakrabarti et al. is directed to a magnetic memory disc which comprises a substrate, a hardening layer and a film made of nonferromagnetic material disposed between the substrate and the hardening layer (col. 1, lines 40-59). As such, the sputtering method taught by Chakrabarti et al. is not employed to ***oxidize and remove the particulate silicon residues*** on the surface of the first conductive line. Therefore, the cited references, singly or in combination, fail to disclose, teach or suggest the claimed operations of oxygen plasma sputtering is employed to ***oxidize and remove the particulate silicon residues*** on the surface of the first conductive line before deposition.

For at least this reason, claim 1 patently defines over the cited art. Since claims 2-13 and 26 depend from claim 1, claims 2-13 and 26 patently define over the cited art for at least the same reasons.

Independent Claim 14

As amended herein, independent claim 14 recites:

> 14. A method of fabricating one time programmable read only memory (OPTROM) device, comprising:
> providing a substrate;
> sequentially forming a stack of p^+-doped silicon layer/titanium silicide/titanium nitride/p^+-doped silicon layer/first dielectric/n-type doped silicon layers on the substrate;
> patterning the stack of p^+-doped silicon layer/titanium silicide/titanium nitride/p^+-doped silicon layer/first dielectric/n-type doped silicon layers along the first direction, thereby turning the stack of p^+-doped silicon layer/titanium silicide/titanium nitride layers into a word line;
> ***etching the stack of p^+-doped silicon layer/first dielectric/n-type doped silicon layers into a memory cell causing particulate silicon residues on the surface of the first conductive line;***
> ***depositing a second dielectric layer overlying the substrate, wherein oxygen plasma sputtering is employed to oxidize and remove the particulate silicon residues on the surface of the first conductive line before deposition;***
> planarizing the second dielectric layer to expose the memory cell; and
> forming a stack of n^+-type doped silicon/ titanium nitride/ titanium silicide /n^+-type doped silicon/n-type doped silicon layers over the second dielectric layer and patterning the same into a bit line, running generally perpendicular to the word line.

(*Emphasis added.*) Claim 1 patently defines over the cited art for at least the reason that the cited art fails to disclose those features emphasized above.

Applicants respectfully submit that Johnson fails to disclose, teach or suggest that particulate silicon residues due to etching process are oxidized and removed by oxygen plasma sputtering before deposition of a second dielectric layer.

Moreover, Applicants respectfully submit that the sputtering method taught by Chakrabarti et al. is not employed to ***oxidize and remove the particulate silicon residues*** on the surface of the first conductive line. Therefore, the cited references, singly or in combination, fail to disclose, teach or suggest the step of oxygen plasma sputtering is employed to ***oxidize and remove the particulate silicon residues*** on the surface of the first conductive line before deposition.

For at least this reason, claim 14 patently defines over the cited art. For at least the same reasons, dependent claims 15-19 and 27 define over the cited art as well.

Conclusion

For the reasons described above, all claims 1-19 and 26-27 are believed to be in condition for allowance, and the Examiner is respectfully requested to pass those claims to issuance. If the Examiner believes a teleconference will expedite the examination of this application, the Examiner is invited to contact the undersigned attorney at 770-933-9500.

A credit card authorization is provided to cover the fee associated with the accompanying RCE application. No additional fee is believed to be due in connection with this submission. If, however, any fee is deemed to be payable, you are hereby authorized to charge any such fee to deposit account 20-0778.

Respectfully submitted ,

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